WHAT IS CLAIMED IS:

1. A method for prefetching data in a multiprocessing computer system comprising:

a cache receiving a request to access a line of data;

determining that a cache miss with respect to the line occurred; and

transmitting a bundled transaction on a system interconnect in response to the cache miss, wherein the bundled transaction combines a request for the line of data and a prefetch request.

2. The method as recited in claim 1 wherein the request corresponding to the line of data is a read request.

3. The method as recited in claim 2 wherein the prefetch request is a prefetch read request.

4. The method as recited in claim 3 wherein the prefetch read request is a request to a sequential cache line.

5. The method as recited in claim 1 wherein the request corresponding to the line of data is an upgrade request.

6. The method as recited in claim 5 wherein the prefetch request is a prefetch upgrade request.

7. The method as recited in claim 6 wherein the prefetch upgrade request is a request to a sequential cache line.

8. The method as recited in claim 1 further comprising a second cache transitioning to a first owner state in response to downgrading from a modified state.

9. The method as recited in claim 8 further comprising a second cache transitioning to a second owner state from the first owner state in response to a read request.

10. A multiprocessing computer system comprising:

a microprocessor configured to convey a request to access a line of data; and

a cache coupled to receive the request, wherein the cache is configured to transmit a bundled transaction on a system interconnect in response to a cache miss, wherein the bundled transaction combines a request for the line of data and a prefetch request.

11. The multiprocessing computer system as recited in claim 10 wherein the request corresponding to the line of data is a read request.

12. The multiprocessing computer system as recited in claim 11 wherein the prefetch request is a prefetch read request.

13. The multiprocessing computer system as recited in claim 12 wherein the prefetch read request is a request to a sequential cache line.

14. The multiprocessing computer system as recited in claim 10 wherein the request corresponding to the line of data is an upgrade request.

15. The multiprocessing computer system as recited in claim 14 wherein the prefetch request is a prefetch upgrade request.

16. The multiprocessing computer system as recited in claim 15 wherein the prefetch upgrade request is a request to a sequential cache line.

17. The multiprocessing computer system as recited in claim 10 further comprising a second cache transitioning to a first owner state in response to downgrading from a modified state.

18. The multiprocessing computer system as recited in claim 17 further comprising a second cache transitioning to a second owner state from the first owner state in response to a read request.